

What is claimed is:

1 1. A method to control the loading of a memory buffer, the memory
2 buffer having a watermark with a first watermark value, the method comprising:
3 receiving an advance indication of a memory service interruption;
4 and
5 based at least in part on the received advance indication of the
6 memory service interruption, modifying the watermark to have a second
7 watermark value different from the first watermark value.

1 2. The method of claim 1, wherein the memory buffer having a
2 watermark has a below-watermark burst size with a first burst size value, the method
3 further comprising:
4 based at least in part on the received advance indication of the
5 memory service interruption, modifying the below-watermark burst size to
6 have a second burst size value different from the first burst size value.

1 3. The method of claim 1, wherein the indication of a memory service
2 interruption includes an advance indication of a memory service interruption having
3 a worst case latency to memory.

1 4. The method of claim 1, wherein the second watermark value is
2 greater than the first watermark value.

1 5. The method of claim 2 wherein the second burst size value is less
2 than the first burst size value.

1 6. The method of claim 2 wherein the second burst size value
2 corresponds to difference between the number of data entries in the memory buffer
3 and the second watermark value.

Summary

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1 7. The method of claim 1, the method further comprising
2 receiving an indication of the termination of the memory service
3 interruption; and
4 based at least in part on the received indication of the termination of
5 the memory service interruption, modifying the watermark to have a third
6 watermark value different from the second watermark value.

1 8. The method of claim 7, wherein the third watermark value equals the
2 first watermark value.

1 9. The method of claim 2, the method further comprising
2 receiving an indication of the termination of the memory service
3 interruption;
4 based at least in part on the received indication of the termination of
5 the memory service interruption, modifying the watermark to have a third
6 value different from the second watermark value; and
7 based at least in part on the received indication of the termination of
8 the memory service interruption, modifying the below-watermark burst size
9 to have a third burst size value different from the second burst size value.

1 10. The method of claim 9, wherein the third watermark value equals the
2 first watermark value, and wherein the third burst size value equals the first burst
3 size value.

1 11. A method to control the loading of a memory buffer, the memory
2 buffer having a watermark with a first watermark value, the method comprising:
3 modifying the watermark to have a second watermark value prior to
4 the occurrence of a memory service interruption, the second watermark value
5 being different than the first watermark value; and
6 modifying the watermark to have a third watermark value subsequent
7 to the occurrence of the memory service interruption, the third watermark
8 value being different than the second watermark value.

1 12. The method of claim 11, wherein the third watermark value equals
2 the first watermark value.

1 13. The method of claim 11, wherein the memory buffer having a
2 watermark with a first watermark value has an below-watermark burst size with a
3 first burst size value, the method further comprising:
4 modifying the below-watermark burst-size to have a second burst size
5 value prior to the occurrence of a memory service interruption, the second
6 burst size value being different than the first burst size value; and
7 modifying the below-watermark burst size to have a third burst size
8 value subsequent to the occurrence of the memory service interruption, the
9 third burst size value being different than the second burst size value.

1 14. The method of claim 13, wherein the first burst size value is equal to
2 the third burst size value.

1 15. An apparatus to control the loading of a memory buffer, comprising:
2 a memory buffer; and
3 a memory controller, coupled to said memory buffer, including
4 a watermark register;
5 a first register, coupled to said watermark register, to store a
6 first watermark value; and
7 a second register, coupled to said watermark register, to store
8 a second watermark value.

1 16. The apparatus of claim 15, wherein the memory controller includes:
2 a below-watermark burst size register;
3 a third register, coupled to said below-watermark burst size
4 register, to store a first below-watermark burst size value; and
5 a fourth register, coupled to said below-watermark burst size
6 register, to store a second below-watermark burst size value.

1 17. The apparatus of claim 15, wherein the memory controller is to:
2 receive an advance indication of a memory service
3 interruption;
4 read the second watermark value from said second register
5 based at least in part on the received advance indication of a memory
6 service interruption; and
7 store the second watermark value in said watermark register.

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1 18. The apparatus of claim 16, wherein the memory controller is to
 2 receive an advance indication of a memory service
 3 interruption;
 4 read the second watermark value from said second register
 5 based at least in part on the received advance indication of a memory
 6 service interruption; and
 7 store the second watermark value in said watermark register;
 8 read the second below-watermark burst size value from said
 9 fourth register based at least in part on the received advanced
 10 indication of a memory service interruption; and
 11 store the second below-watermark burst size value in said
 12 below-watermark burst size register.

1 19. A system to process video signals, the system comprising:
 2 a processor;
 3 a memory, coupled to said processor;
 4 a memory buffer, coupled to said memory; and
 5 a memory controller, coupled to said memory buffer, including
 6 a watermark register;
 7 a first register, coupled to said watermark register, to store a
 8 first watermark value; and
 9 a second register, coupled to said watermark register, to store
 10 a second watermark value.

1 20. The system of claim 19, wherein the memory controller is to:
 2 receive an advance indication of a memory service
 3 interruption;
 4 read the second watermark value from said second register
 5 based at least in part on the received advance indication of a memory
 6 service interruption; and
 7 store the second watermark value in said watermark register.

1 21. A computer-readable medium storing a plurality of instructions to be
2 executed by a processor to control a memory buffer having a watermark with a first
3 watermark value and a below-watermark burst size with a first burst size value, said
4 plurality of instructions comprising instructions to:

5 receive an advance indication of a memory service interruption; and
6 based at least in part on the received advance indication of the
7 memory service interruption, modify the watermark to have a second
8 watermark value different from the first watermark value.

1 22. The computer-readable medium of claim 21, further comprising
2 instructions to:

3 based at least in part on the received advance indication of the
4 memory service interruption, modify the below-watermark burst size to have
5 a second burst size value different from the first burst size value.

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